

Figure 1 illustrates a five-step photolithography process:

- Step 1:** A substrate (8) is coated with a photoresist layer (12).
- Step 2:** A mask (10) is placed on the photoresist, and UV light (16) is projected through it, creating a latent image (18).
- Step 3:** The photoresist is developed, removing the unexposed areas.
- Step 4:** A material of interest (14) is deposited over the entire surface, including the mask.
- Step 5:** The mask and the unexposed photoresist are removed, leaving the material of interest (14) patterned on the substrate (8).

Legend:

- Substrate (8)
- Photoresist (12)
- Mask (10)
- Material of Interest (14)
- UV light (16)

Figure 1.3: Lift-off processing

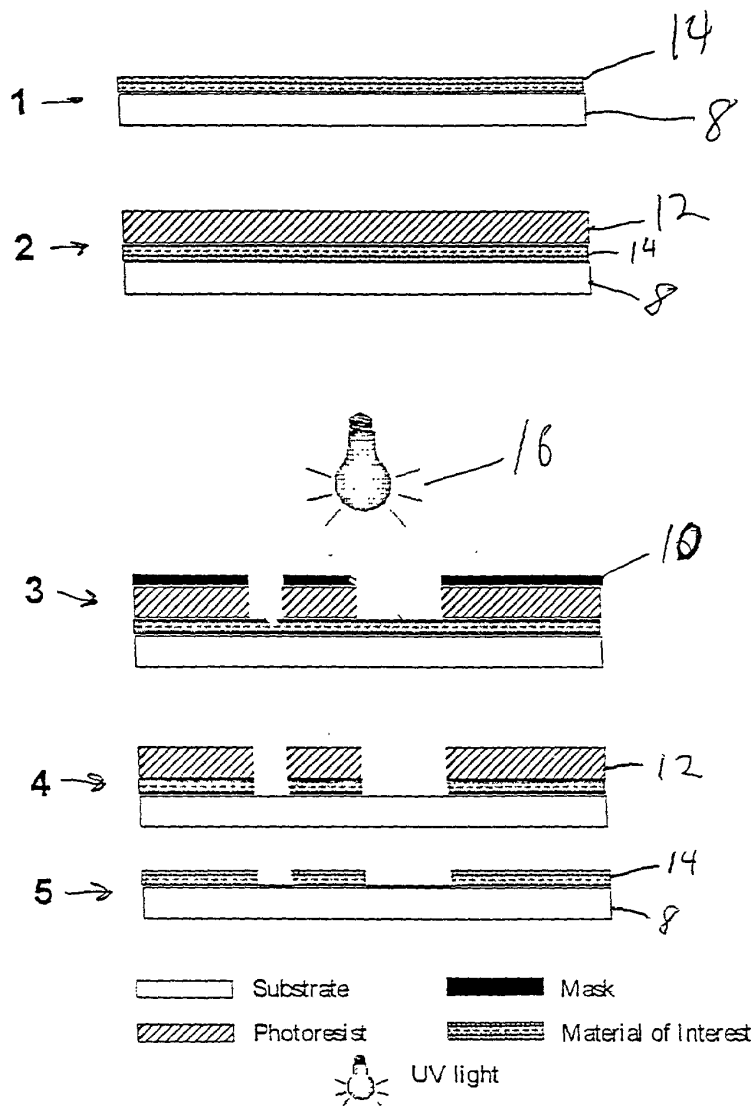
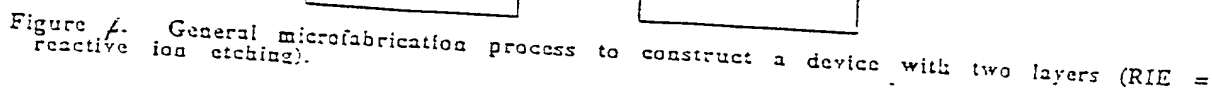


Fig 2

Figure 1.4: Etching procedure

[illegible]

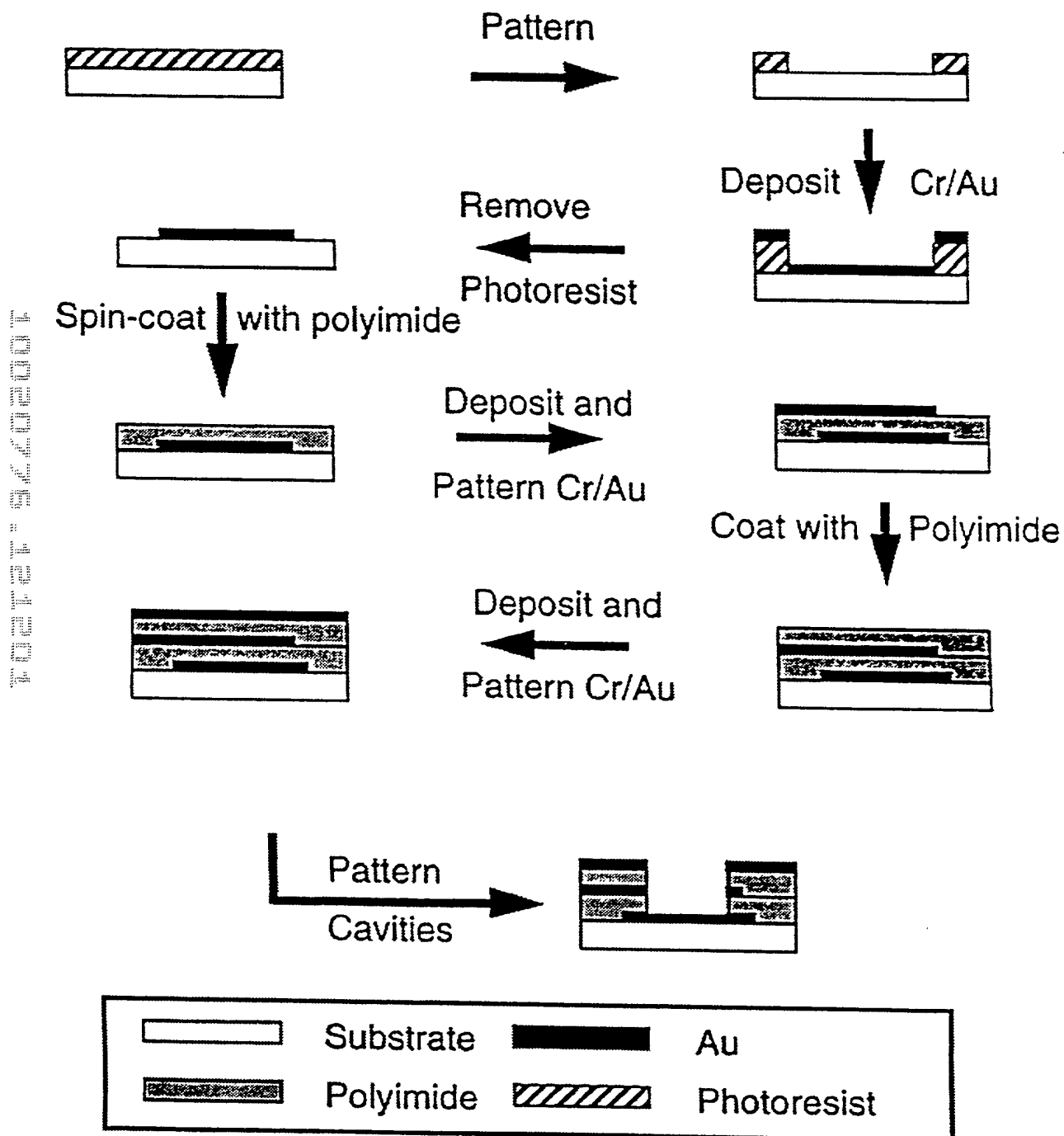
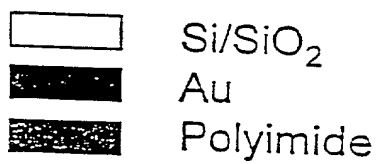
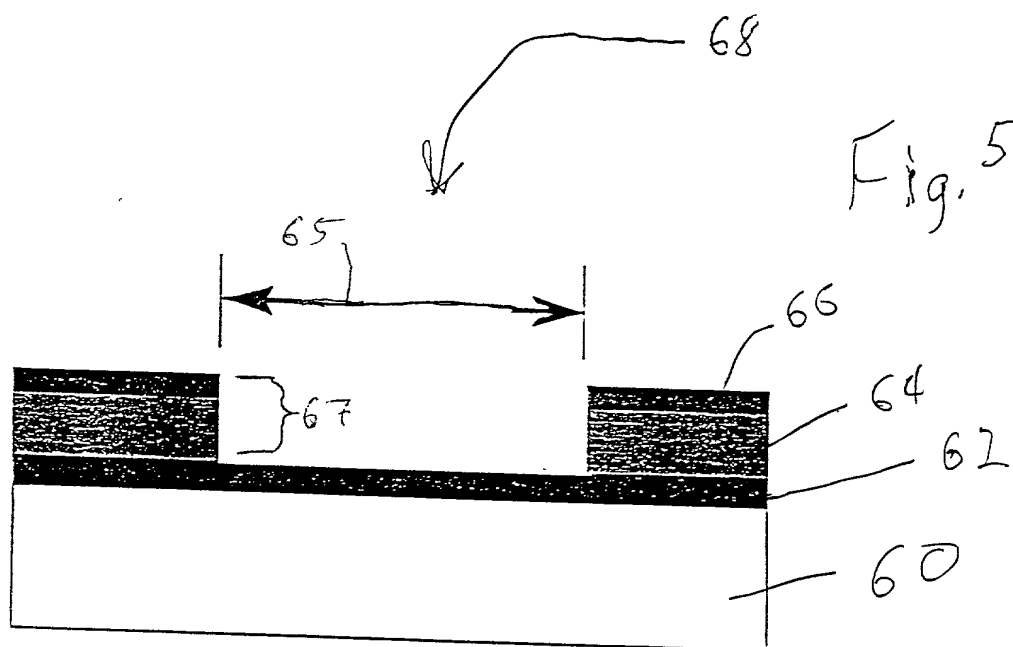


Figure 4. Schematic of the fabrication procedure for the 5-layer microcavity device.

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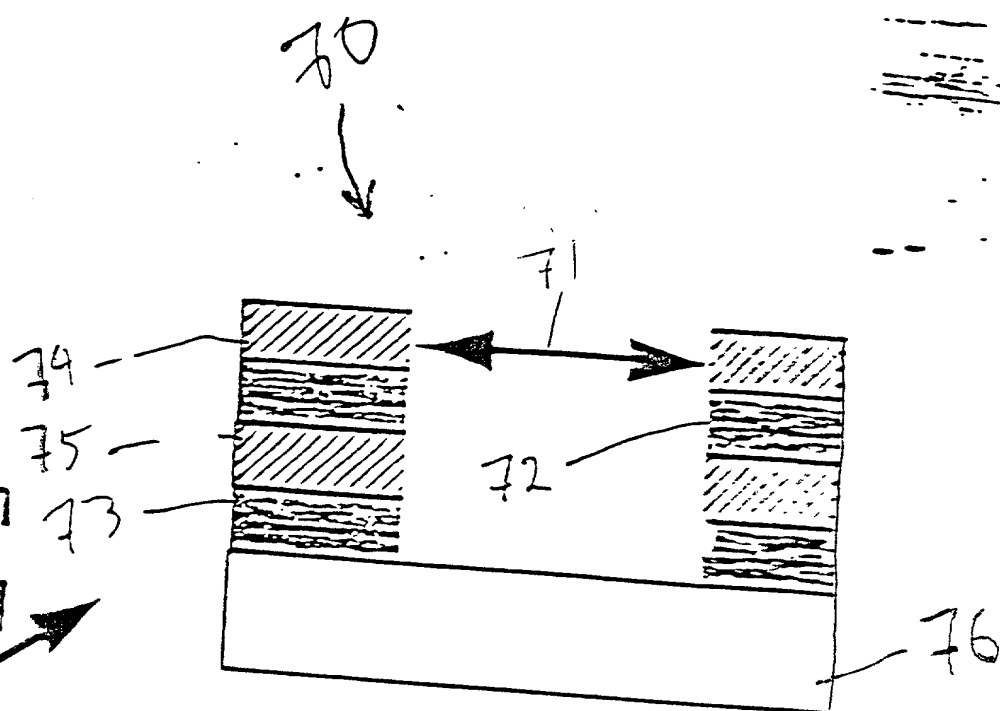


Fig. 6

A Disk and a Band Electrode

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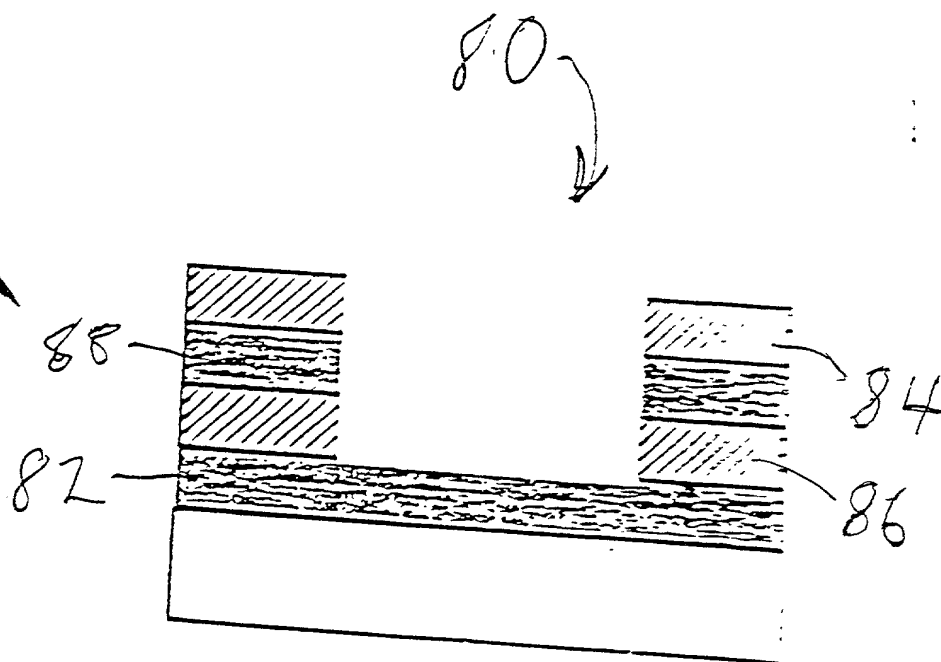


Fig. 7

Two Band Electrodes

$$0.001 \mu\text{m} \leq h \leq 500 \mu\text{m}$$

Fig 9

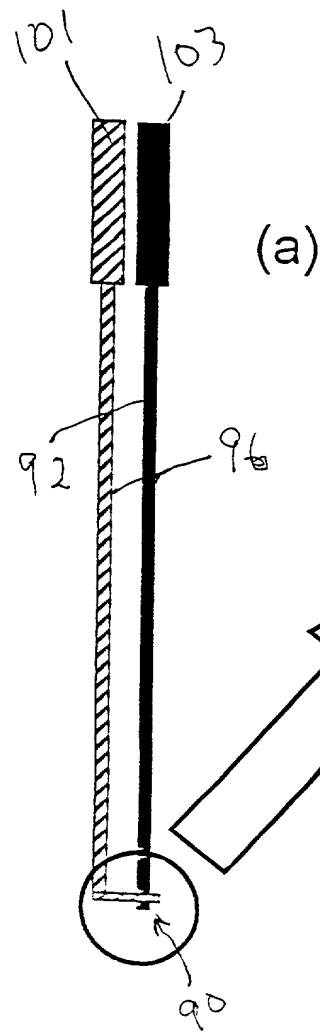
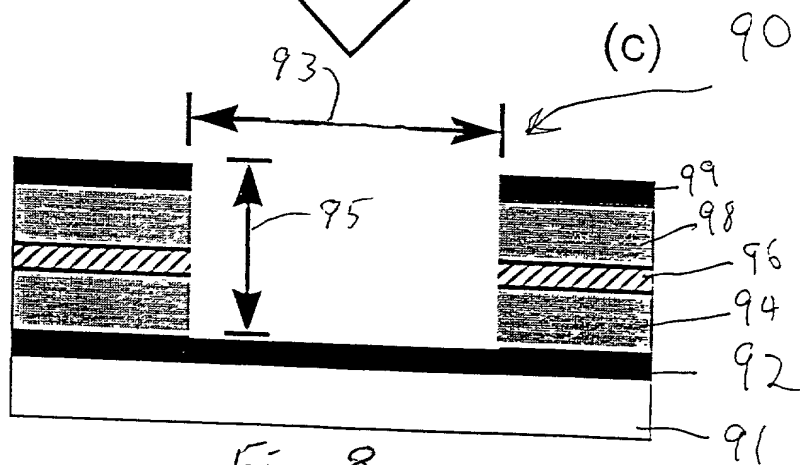
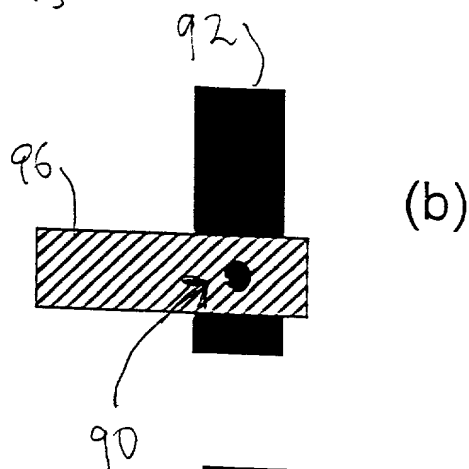


Fig 10



Figure


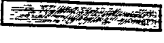
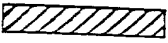
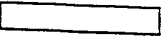
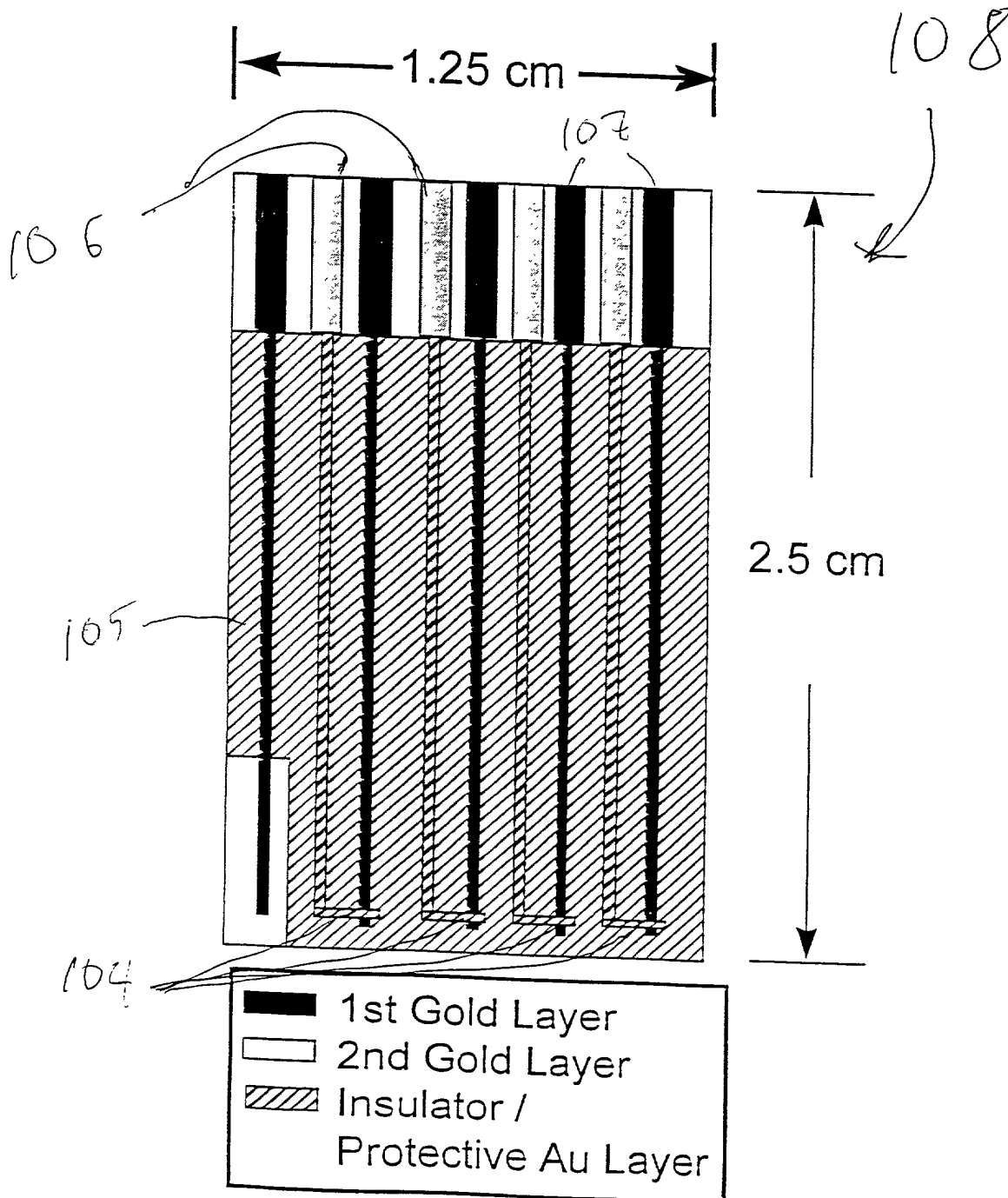
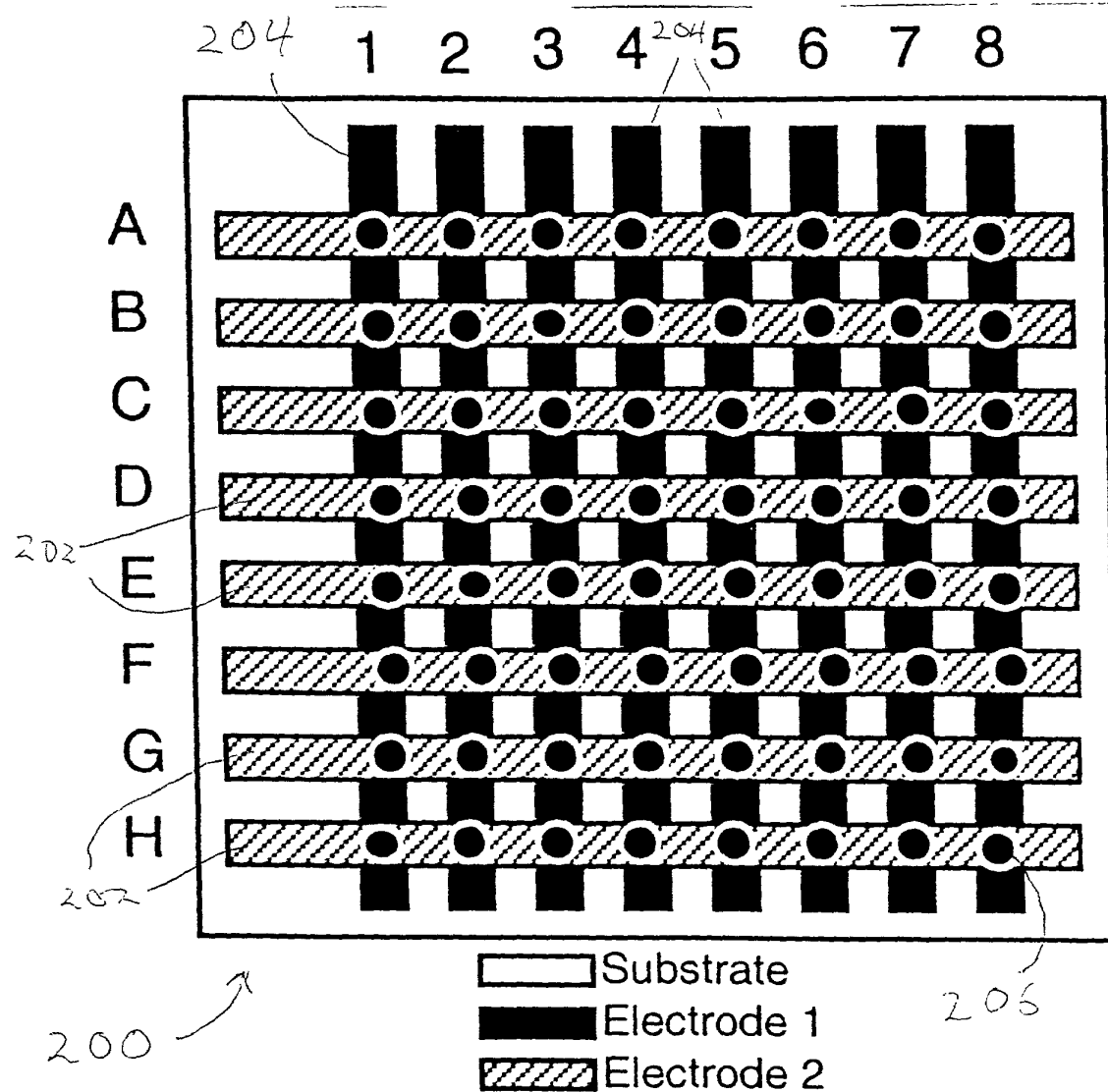
	Au		Polyimide
	Au (Layer 3)		Substrate

Fig 11



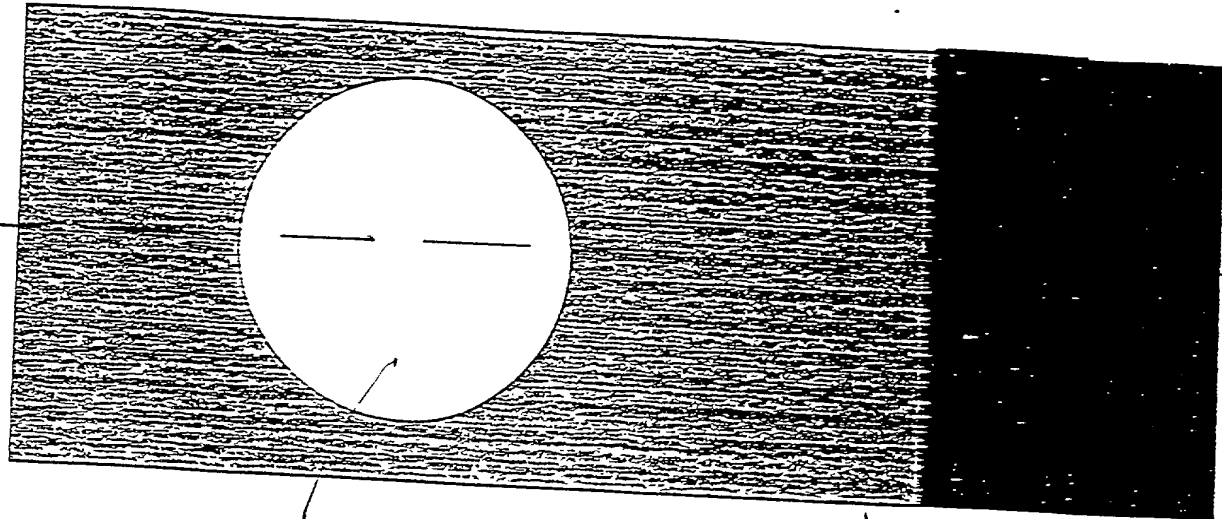


8 array for multi-small volume microelectrochemical analysis.

Fig. 12

Fig. 13

Top View



Cross-sectional View

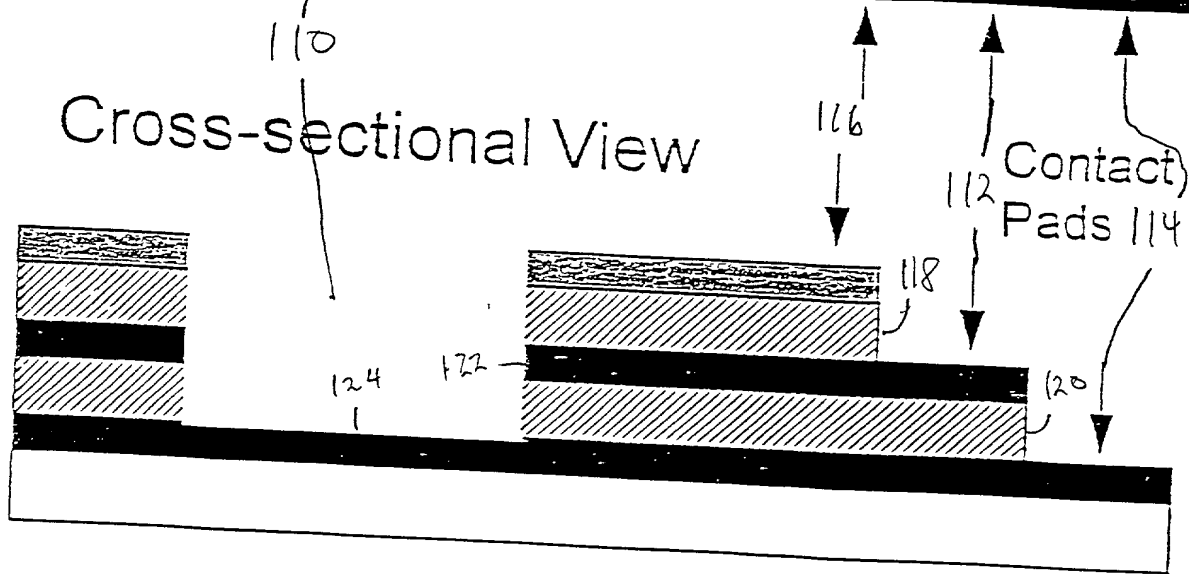


Fig. 14





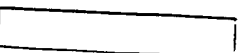
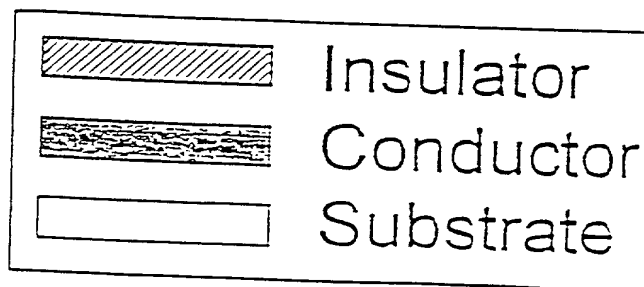
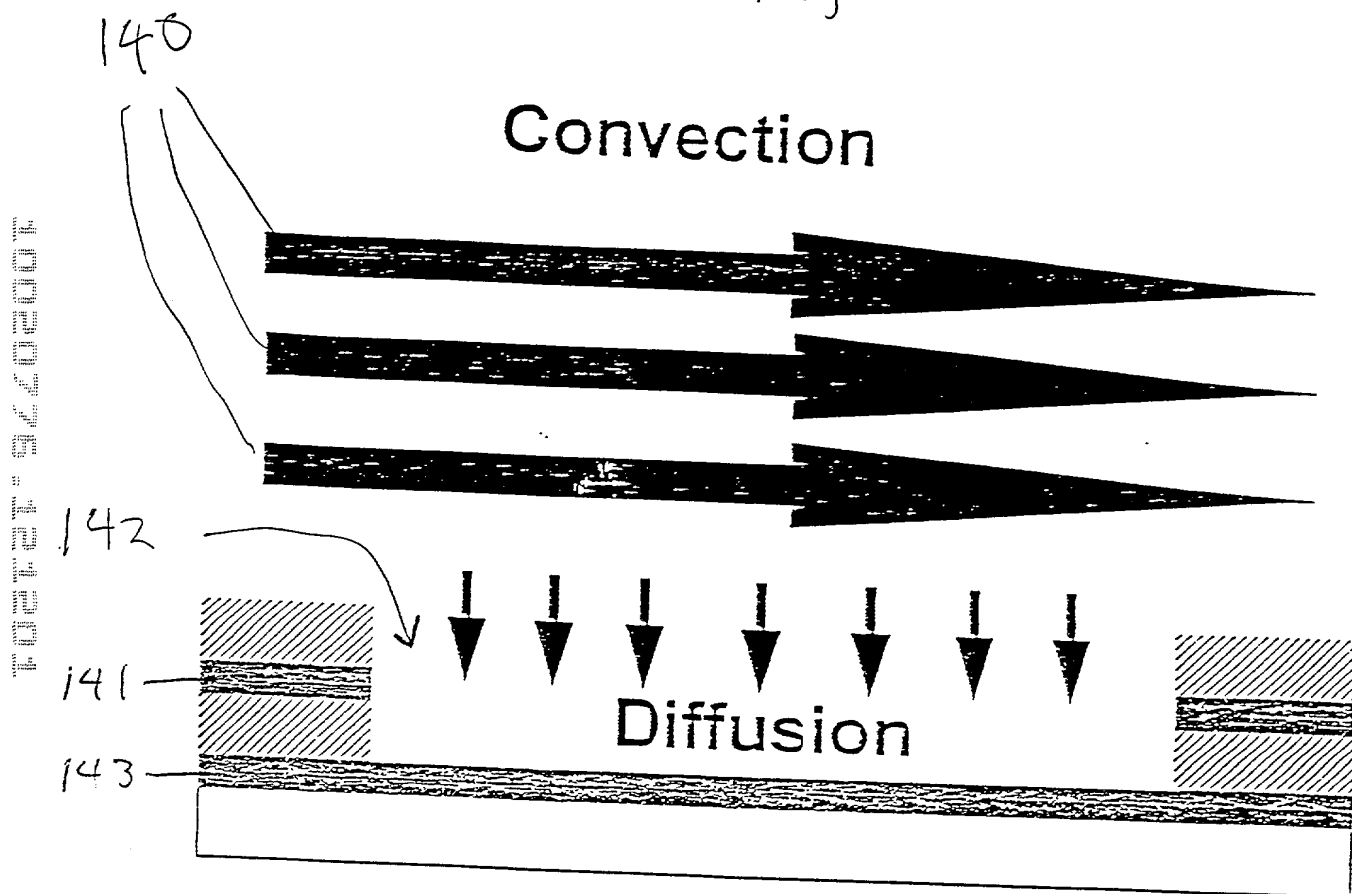
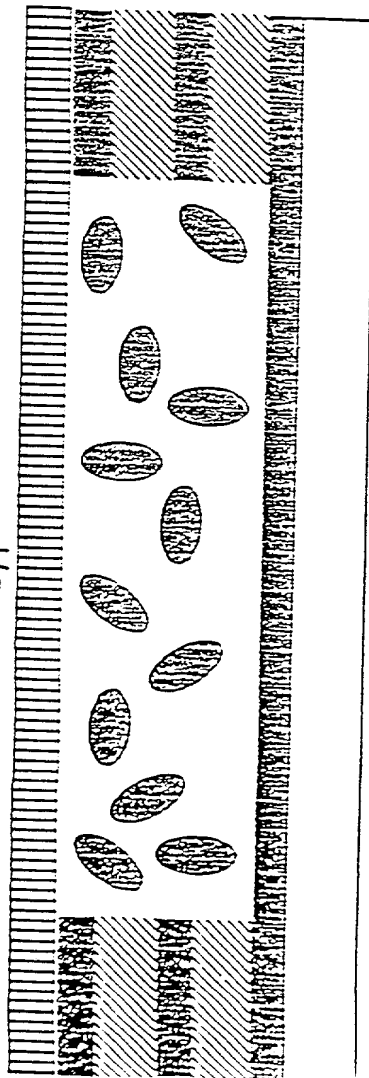
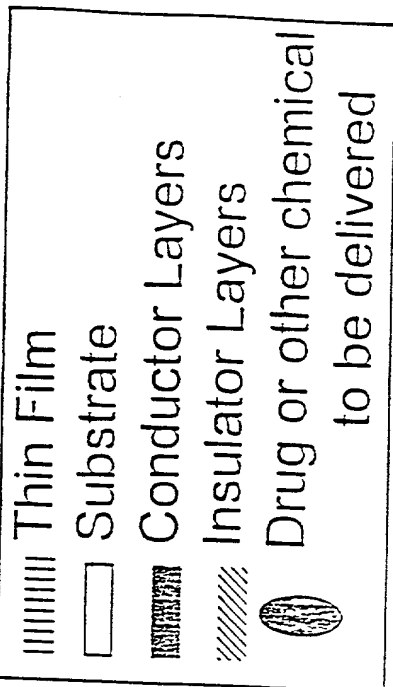
	Insulator Layers
	1st Conductor Layer
	2nd Conductor Layer
	3rd Conductor Layer
	Substrate

Fig 15



11



Osmotic Change, or
Applied Potential, or
Chemical Disruption of Film

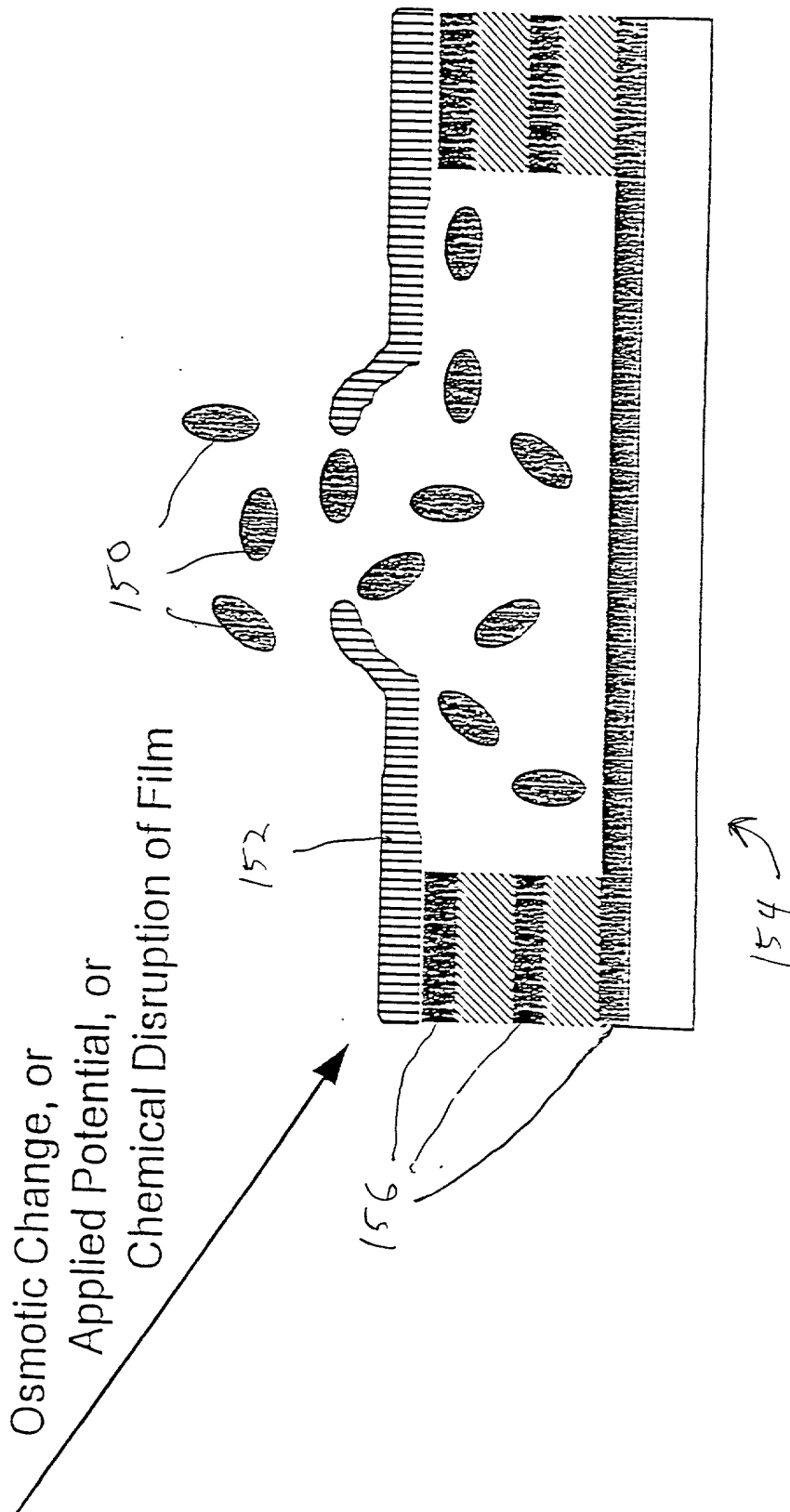
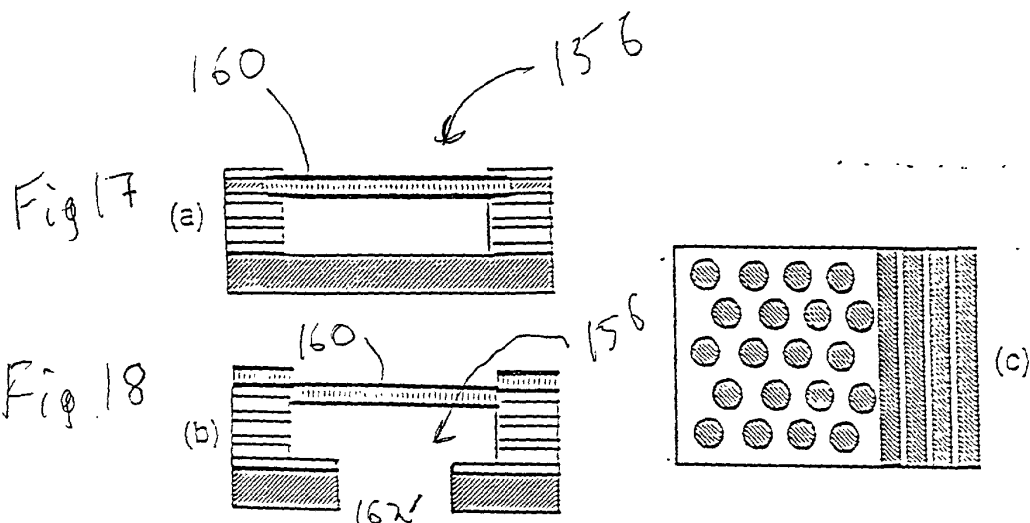


Fig. 16



Other possible target structures for three-dimensional microfabricated devices. *On left:* Cross sections with suspended bilayers; Au band electrodes, represented in light gray. (a) Edges of bilayer anchored by alkanethiol-derivatized inner edges of Au layers in an etched region of insulator (white); bottom of well is lined with an insulator layer. (b) Same as Figure 4, but with a hole at its base to minimize osmotic effects (substrate here is Si_3N_4 for this purpose). *On right:* Top view of a multiple-well array. Each circle represents a single cavity ($1\text{ }\mu\text{m}$ to $100\text{ }\mu\text{m}$) over which a bilayer will be assembled. Each contact pad accesses a different level of conductor.

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Fig 19

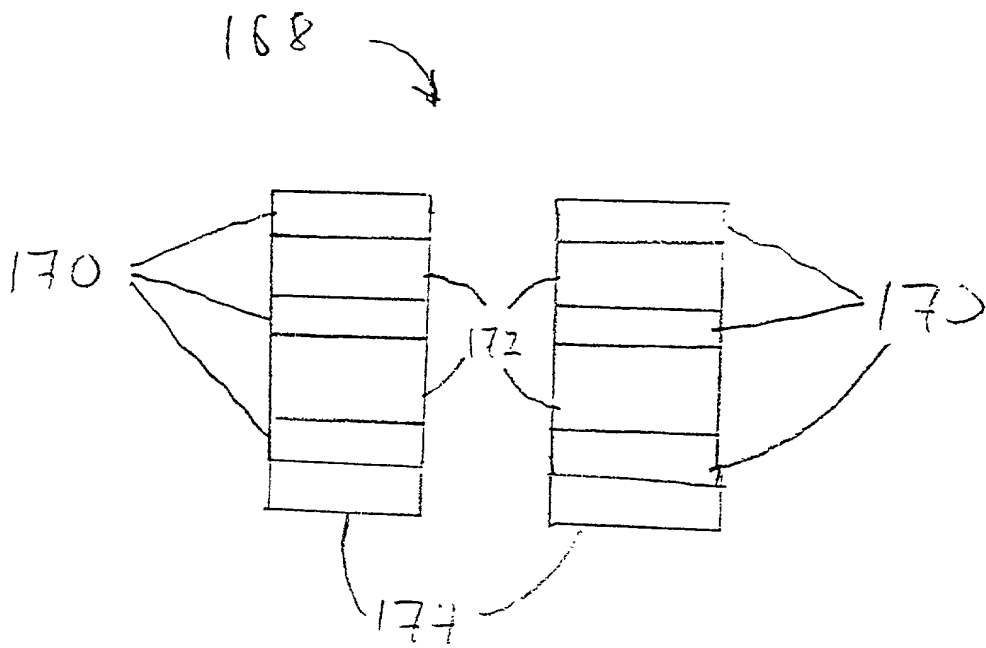


Fig. 20

